Routing in Optical Multistage Interconnection Networks: a Neural Network Solution *

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Abstract

There has been much interest in using optics to implement computer interconnection networks. However, there has been little discussion of any routing methodologies besides those already used in electronics. In this paper, a neural network routing methodology is proposed that can generate control bits for a broad range of optical multistage interconnection networks (OMINs). Though we present no optical implementation of this methodology, we illustrate its control for an optical interconnection network. These OMINs can be used as communication media for distributed computing systems. The routing methodology makes use of an Artificial Neural Network (ANN) that functions as a parallel computer for generating the routes. The neural network routing scheme can be applied to electrical as well as optical interconnection networks. However, since the ANN can be implemented using optics, this routing approach is especially appealing for an optical computing environment. Although the ANN does not always generate the best solution, the parallel nature of the ANN computation may make this routing scheme faster than conventional routing approaches, especially for OMINs that have an irregular structure. Furthermore, the ANN router is fault-tolerant. Results are shown for generating routes in a 16×16, 3-stage OMIN.

1 Introduction

Artificial Neural Networks (ANNs) of the type that were described by Hopfield [13] are capable of finding good solutions for certain optimization problems [14]. Furthermore, these ANNs can also solve certain constraint satisfaction problems. Constraint satisfaction problems can often be modeled as optimization problems that have numerous correct solutions that are of equal value.

The routing of a set of messages through a multistage interconnection network (MIN) can be modeled as a constraint satisfaction problem. MINs are often used in parallel processing

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and distributed computing systems and are currently the subject of much interest in the parallel computing community. Generating the control bits that define the routes for the MIN may be a time consuming process that can cause a bottleneck in the system.

An ANN has been designed that can potentially solve the problem faster than conventional means. This neural network solution, however, is only applicable to a particular class of interconnection network. The interconnection network must be constructed out of layers of complete or incomplete crossbar switches. There is no restriction on the connections between successive layers. There can be no feedback connections and no connections that skip a layer of the interconnection network. Such interconnection networks are often called *leveled* interconnection networks. We shall call them MINs.

Electronic multistage interconnection networks (EMINs) are usually considered to be 2-dimensional, while optical multistage interconnection networks (OMINs) are generally 3-dimensional. However, the structures of both EMINs and OMINs are such that the routing problem is similar in both cases. In fact, a 3-dimensional MIN routing problem can be directly mapped to a 2-dimensional MIN routing problem.

The model being considered has a set of input ports and a set of output ports that are connected via the MIN. The problem that is addressed is a point-to-point communication problem. That is to say, no broadcasting is allowed. Additionally, the circuit switching problem is being considered: for an input port to communicate with an output port, the entire route has to be established and maintained for a certain period of time. There is no stage-by-stage passing of message packets through the MIN. At the beginning of each message cycle, an input port may decide that it wants to communicate with an output port. For each message cycle there is a set of desired messages. The problem is to generate control bits for the MIN given the message set.

Figure 1 contains a diagram of a communication system with a neural network router. The neural network router is discussed in [8, 9]. In these references the neural network router is applied to an EMIN routing problem. The very same methodology, however, can be applied to a 3-dimensional OMIN problem by collapsing the 3-dimensional problem down to a 2-dimensional problem. The ANN mentioned above is the crucial component of the neural

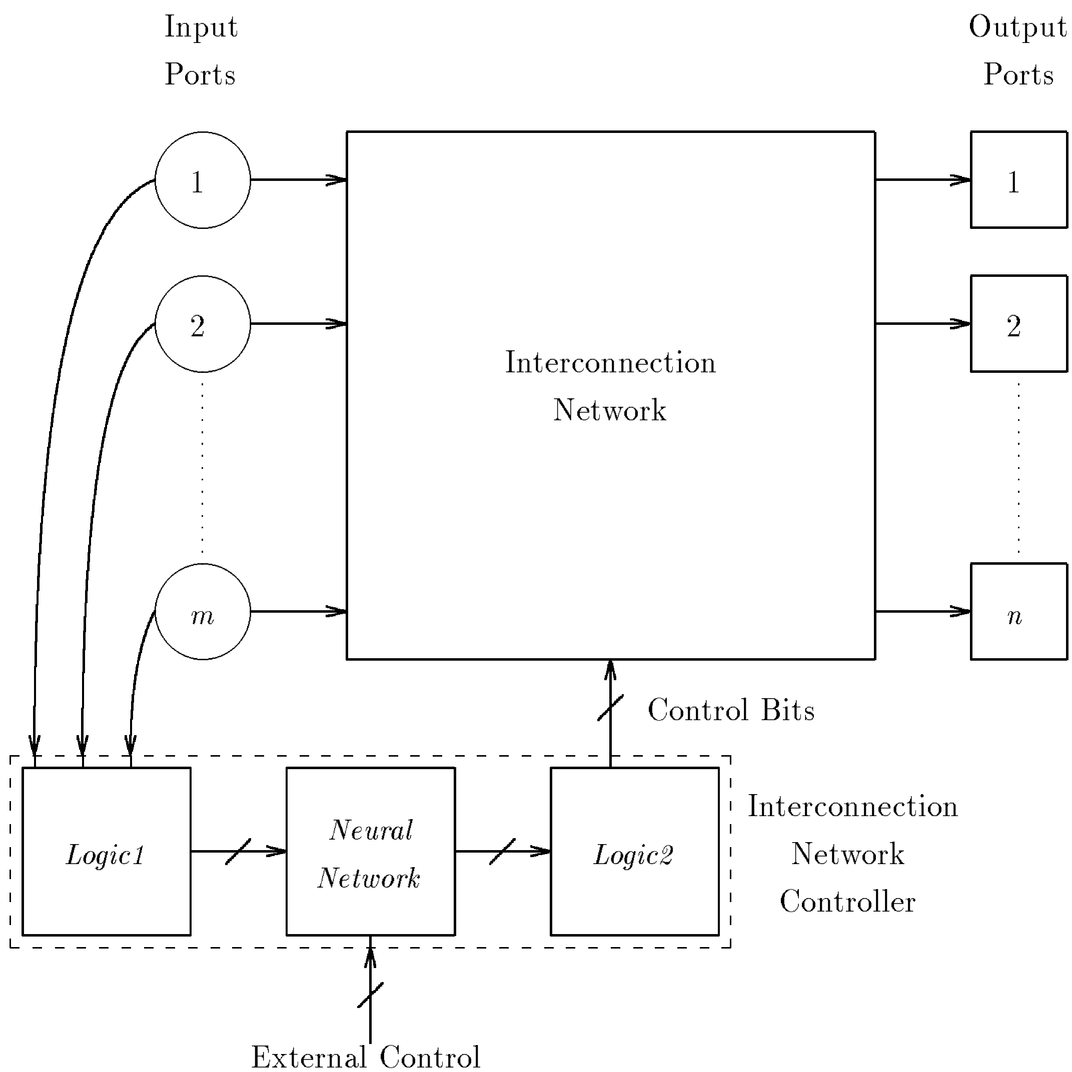

Figure 1: The communication system with a neural network router.

network router. Since Hopfield model neural networks can be constructed efficiently using an optical system [4, 5], the neural network routing methodology is particularly appealing for an optical computing environment.

The neural network router in Figure 1 has two logic blocks to interface the neural network with the rest of the communication system. The logic block *Logic1* converts the desired message set into a language the neural network can understand, namely bias currents. The logic block *Logic2* is required to convert the routing array solution of the neural network into a crosspoint form that the interconnection network can understand. The construction of these logic blocks should be a straightforward process.

Further information on interconnection networks can be found in [1, 15]. There has already been some interesting work done on utilizing Hopfield model neural networks to facilitate communication through interconnection networks. Both the routing problem and the maximization of throughput problem have been addressed for certain interconnection networks [2, 3, 6, 9, 10, 18, 20, 19, 22, 24, 26].

2 Optical Interconnection Networks

There has been much interest in using optical technology for implementing interconnection networks and switches; for a collection of such work see [7]. Our concern will be on optical multistage interconnection networks [12, 17, 21, 16]

Consider the interconnection network in Figure 2. It is an example of a 16×16, 3 stage OMIN. The basic building block is a 4×4 optical crossbar switch [23, 11]. The OMIN has 12 of these switches. Each crossbar switch in the OMIN is connected to each crossbar switch in the neighboring stages. This MIN is capable of routing any input/output permutation. Its construction is similar to that of the standard Benes network [1, 25], although the Benes network's basic building block is a 2×2 crossbar switch. However, the OMIN has the same type of recursive structure as the standard Benes network.

The 3-dimensional routing problem will now be reduced to a 2-dimensional routing problem. This concept was mentioned in Section 1. In Figure 3, there is a 2-dimensional representation of the 3-dimensional MIN from Figure 2. The MIN in Figure 3 is exactly the same as the MIN in Figure 2.

3 The Routing Representation

A routing representation for routes in a MIN will now be constructed. This representation will be called the routing array. In Section 4, the appropriate ANN structure will be described. The neural network will be in a state of minimal energy when the neuron outputs directly represent a legal routing array.

Figure 3 shows two routes, namely a 2-12 route and a 13-16 route. Only one of the many possible routing solutions for these two desired connections is shown.

Each message route will have a corresponding routing matrix. For example, the routing matrix for the 2-12 message in Figure 3 is shown as the leftmost table in Table 1. The columns of a routing matrix represent the stages of the interconnection network, while the rows represent the output ports for each stage of the interconnection network. If $a_{i,j} = 1$, the message is routed through output port i of stage j. Having $a_{i,j} = 0$ implies that the message is *not* routed through output port i of stage j. Thus, the 2-12 message is routed through output port 4 of stage 1, output port 15 of stage 2, and output port 12 of stage 3. The routing matrix for the 13-16 message is shown as the rightmost table in Table 1.

The routing array for the set of messages is simply constructed by treating each routing matrix as a "slice" and constructing a "loaf". The routing array is a 3-dimensional representation of a set of routes, and each slice of the array represents a single route. For our example, there are two messages to be routed so the routing array will have two slices. In general, if a system has m input ports, as in Figure 1, there can be m slices in the routing array.

Each element of the routing array now has three indices. If element $a_{i,j,k}$ is equal to 1 then message i is routed through output port k of stage j. We say $a_{i,j,k}$ and $a_{l,m,n}$ are in the same *row* if $i = l$ and $k = n$. They are in the same *column* if $i = l$ and $j = m$. Finally, they are in the same *rod* if $j = m$ and $k = n$.

A legal routing array will satisfy the following three constraints:

1. one and only one element in each column is equal to 1.

2. the elements in successive columns that are equal to 1 represent output ports that can be connected in the interconnection network.

3. no more than one element in each rod is equal to 1.

The first restriction ensures that each message will be routed through one and only one output port at each stage of the interconnection network. The second restriction guarantees that each message will be routed through a legal path in the interconnection network.

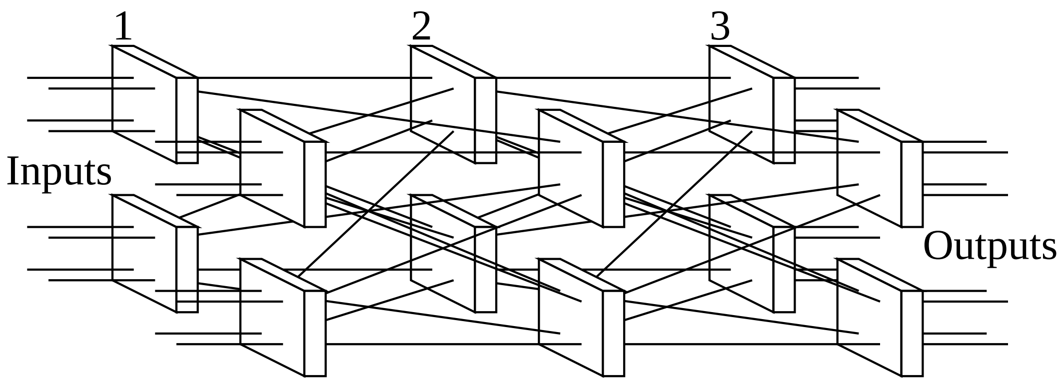

Figure 2: A 3-dimensional optical interconnection network using 12 4×4 crossbar switches.

The third restriction resolves any resource contention in the interconnection network. In other words, only one message can use a certain output port at a certain stage in the interconnection network. When all three of these constraints are met, the routing array will provide a legal routing for each message in the message set.

4 The Neural Network Router

In this section we describe the construction of an ANN (of the type examined by Hopfield) in which each neuron directly represents an element in the routing array for an interconnection network and message set. The ANN has a three-dimensional structure just like the routing array. Each $a_{i,j,k}$ of a routing array is represented by the output voltage of a neuron, $V_{i,j,k}$. It will be shown later in this section that a neuron will only be connected to other neurons that are in its neighborhood. That is, the ANN is not totally connected. At the beginning of a message cycle, the neurons have a random output voltage. If the ANN settles in one of the global minima, the problem will have been solved.

A synchronous Hopfield model neural network is used [14, 13]. The value of τ, from [14], is set to 1.

The ANN is forced into stable states that are the local minima of the energy equation:

$$E = -\frac{1}{2}\sum_{i=1}^{N}\sum_{j=1}^{N} T_{ij}V_iV_j - \sum_{i=1}^{N} V_iI_i \tag{1}$$

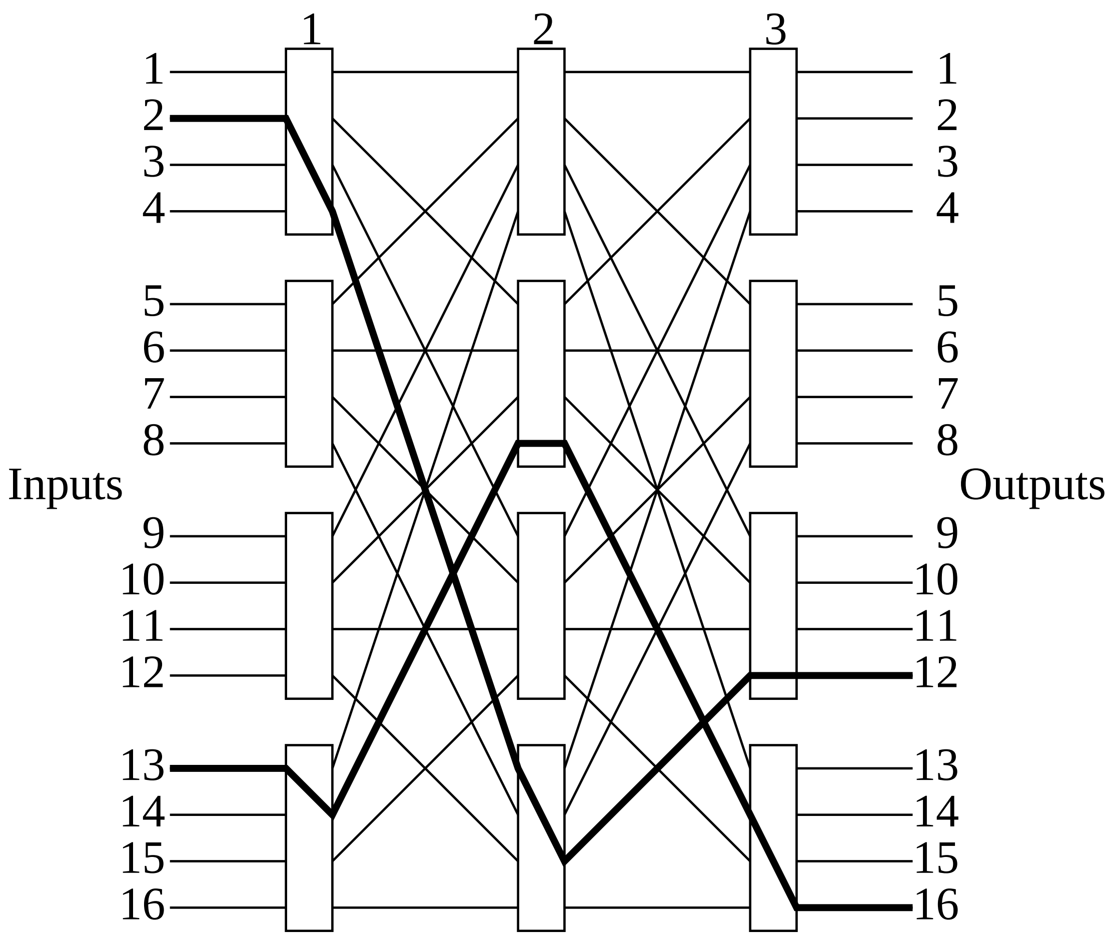

Figure 3: A 2-dimensional representation of the interconnection network in Figure 2. This interconnection network has a 2-12 connection and a 13-16 connection.

		Stage		
		1	2	3
	1	0	0	0
	2	0	0	0
	3	0	0	0
	4	1	0	0
	5	0	0	0
	6	0	0	0
Output	7	0	0	0
Port	8	0	0	0
	9	0	0	0
	10	0	0	0
	11	0	0	0
	12	0	0	1
	13	0	0	0
	14	0	0	0
	15	0	1	0
	16	0	0	0

		Stage		
		1	2	3
	1	0	0	0
	2	0	0	0
	3	0	0	0
	4	0	0	0
	5	0	0	0
	6	0	0	0
Output	7	0	0	0
Port	8	0	1	0
	9	0	0	0
	10	0	0	0
	11	0	0	0
	12	0	0	0
	13	0	0	0
	14	1	0	0
	15	0	0	0
	16	0	0	1

Table 1: Matrix representations for the 2-12 and 13-16 connections shown in Figure 3.

Now an energy function is constructed such that the neural network will be in a global minima when it directly represents a legal routing array. The energy function has four components that are shown here:

$$E_1 = \frac{A}{2} \sum_{m=1}^{M} \sum_{s=1}^{S-1} \sum_{p=1}^{P} V_{m,s,p}(-V_{m,s,p} + \sum_{i=1}^{P} V_{m,s,i}) \tag{2}$$

$$E_2 = \frac{B}{2} \sum_{s=1}^{S-1} \sum_{p=1}^{P} \sum_{m=1}^{M} V_{m,s,p}(-V_{m,s,p} + \sum_{i=1}^{M} V_{i,s,p}) \tag{3}$$

$$E_3 = \frac{C}{2} \sum_{m=1}^{M} \sum_{s=1}^{S-1} \sum_{p=1}^{P} (-2V_{m,s,p} + V_{m,s,p}(-V_{m,s,p} + \sum_{i=1}^{P} V_{m,s,i})) \tag{4}$$

$$\begin{aligned} E_4 \quad = \quad & D \sum_{m=1}^{M} \left[\sum_{s=2}^{S-1} \sum_{p=1}^{P} \sum_{i=1}^{P} d(s,p,i) V_{m,s-1,p} V_{m,s,i} \right. \\ & \left. + \sum_{j=1}^{P} (d(1,\alpha_m,j) V_{m,1,j} + d(S,j,\beta_m) V_{m,S-1,j}) \right] \end{aligned} \tag{5}$$

A, B, C, and D are arbitrary positive constants. E_1 and E_3 handle the first constraint in the routing array. E_4 deals with the second constraint. E_2 ensures the third. From the equation for E_4, the function $d(s1, p1, p2)$ represents the "distance" between output port $p1$ from stage $s1-1$ and output port $p2$ from stage $s1$. If $p1$ can connect to $p2$ through stage $s1$, then this distance can be set to zero. If $p1$ and $p2$ are not connected through stage $s1$, then the distance can be set to one. Also, α_m is the source address of message m, while β_m is the destination address of message m.

The entire energy function is:

$$E = E_1 + E_2 + E_3 + E_4 \tag{6}$$

Solving for the connection and bias current values as shown in Equation 1 results in the following equations:

$$\begin{aligned} T_{(m1,s1,p1),(m2,s2,p2)} &= -(A+C)\delta_{m1,m2}\delta_{s1,s2}(1-\delta_{p1,p2}) \\ &\quad -B\delta_{s1,s2}\delta_{p1,p2}(1-\delta_{m1,m2}) \\ &\quad -D\delta_{m1,m2}[\delta_{s1+1,s2}d(s2,p1,p2) + \delta_{s1,s2+1}d(s1,p2,p1)] \end{aligned} \tag{7}$$

$$I_{m,s,p} = C - D[\delta_{s,1}d(1,\alpha_m,p) + \delta_{s,S-1}d(S,p,\beta_m)] \tag{8}$$

$\delta_{i,j}$ is a Kronecker delta ($\delta_{i,j} = 1$ when $i = j$, and 0 otherwise). The connection values from Equation 7 are well defined for a given MIN. That is, once the MIN is designed, the neural network and all of its inter-neuron connections can be calculated. When different groups of input-output ports need to be connected, it is only the input bias currents of boundary neurons that are affected. Equation 8 quantifies that change.

If the circuit implementation of the ANN from [13] is utilized, changing to a new set of desired messages corresponds to reducing the input bias currents to illegal nodes in the first and last stages of the ANN. The connectivity matrix is defined totally by the MIN that is chosen, and so the conductances need not change.

If the user has the ability to make the output of a rod of neurons equal to zero or give a rod of neurons a large negative input bias current, then the neural network can provide a fault-tolerant routing scheme. For example, if an output port in some stage of the interconnection network is faulty, the user could set the rod of neurons that represents that output port to zero. The rest of the neural network can operate exactly as it did before. Neither the structure nor the weights need to be changed. Similarly, this routing methodology could tolerate faulty input ports and broken buses. However, the user must know if a fault exists and where it exists in the MIN.

5 Simulation Results

A synchronous ANN was simulated and the results are shown in Table 2 for routing in the OMIN shown in Figure 2. For the OMIN shown in Figure 2, the neural network router contained $16 \times 16 \times 2 = 512$ neurons. Each row of the table gives the results for a set of 1000 message cycles. The M represents the number of messages that are to be routed in each message cycle. The message pairs are generated randomly with no input port or output port conflicts allowed. The CS% represents the percentage of *complete successes*, where a complete success occurs when each message in the message set is successfully routed. The SM% is the percentage of *successful messages*, that is messages that are routed correctly regardless of whether there has been a completely successful routing for the entire message set. Thus, CS% $\leq$ SM%. A message is considered to have been routed successfully when the neural network provides it with a legal routing and when the message has no contention with any other message for an output port in any stage of the MIN. Finally, EM represents the expected number of messages routed in each message cycle. It is obtained by multiplying the first and third columns and dividing by 100. A graph of EM versus M is shown in Figure 4.

For the OMIN shown in Figure 2, any I/O permutation is possible. Thus, any message that is not routed correctly implies a failure in the neural network solution, not a limitation in the MIN. For the distributed computing system that is used as a model in this paper, any input port that can not communicate with an output port in a message cycle may try to communicate with the same output port in the next message cycle. With this model, a very high-speed routing system that does not necessarily establish all routes possible from a message set can still outperform a slower algorithm that can establish all possible routes. A good implementation of the neural network router may have speed advantages over deterministic routing algorithms. Furthermore, there are many MINs that will have

M	CS%	SM%	EM
1	100.0	100.0	1.00
2	100.0	100.0	2.00
3	100.0	100.0	3.00
4	100.0	100.0	4.00
5	100.0	100.0	5.00
6	99.4	99.9	5.99
7	97.8	99.7	6.98
8	93.6	99.2	7.94
9	84.9	98.2	8.84
10	75.9	97.4	9.74
11	58.8	95.8	10.54
12	42.9	93.8	11.26
13	25.6	91.4	11.88
14	17.1	89.2	12.49
15	11.3	86.2	12.93
16	9.4	82.7	13.23

Table 2: Simulation results for the MIN shown in Figure 2.

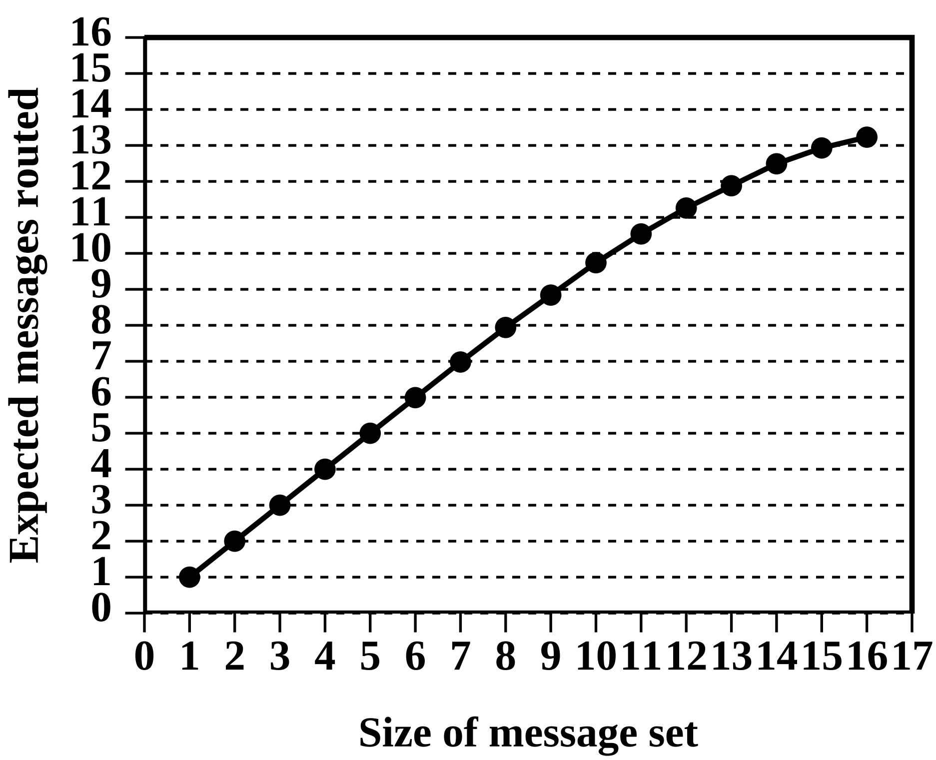

Figure 4: Routing results from Table 2. EM versus M.

no effective deterministic routing algorithms. For MINs such as these, the neural network router may be particularly useful.

For the purposes of the simulations, A, C, and D from Equations 7 and 8 were all set to 3.0. B was set to 6.0. The performance of the neural network router is highly dependent upon these parameters. The parameters that were chosen here were arrived at experimentally. There is no claim as to their optimality. The analog neural network was simulated with a digital computer. The output values of the neurons were updated every 0.1 time units. The initial output values of the neurons were in the range (0.45,0.55) and were uniformly distributed.

The simulations show that increasing the number of messages degrades the performance of the system. Other simulations show that the performance also degenerates as the number of stages increases and as the number of connections between stages increases.

6 Conclusions

A neural network routing methodology was presented that is capable of providing control bits to an optical multistage interconnection network (OMIN). It was shown how the 3-dimensional OMIN can be reduced to a 2-dimensional MIN, making the neural network routing solution possible. This routing method is valid for a wide range of OMINs that have a certain structure. It was shown that the routing method is fault-tolerant. Once the OMIN is chosen, the routing neural network can be constructed and the weights never have to change. For a new message set, only certain boundary bias currents need to be varied.

The usefulness of this routing method depends on the speed of the Hopfield neural network as well as other requirements of the system. The fact that a Hopfield neural network can be readily constructed in an optical computing environment makes the neural network routing approach quite attractive for OMIN routing problems.

The routing performance degrades as the MIN size increases and as the number of messages in a message cycle increases. Preliminary results show that the performance of the neural network router will fall off considerably as the number of stages in a MIN increase. Depending on the implementation of the neural network router, the routing method described in this paper may have advantages over other routing methods in terms of speed. Furthermore, the neural network routing methodology can be applied to many irregular OMINs that have no known deterministic routing scheme that is better than an exhaustive search. Thus, the neural network routing methodology may be most suitable for establishing routes for irregular OMINs and OMINs that do not have self-routing capabilities.

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